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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/912,500	07/26/2001	Haeng-Seon Kim	06192.0197.NPUS00	6260

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EXAMINER
LESPERANCE, JEAN E

ART UNIT	PAPER NUMBER
2674	6

DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/912,500	KIM, HAENG-SEON	
	Examiner	Art Unit	
	Jean E Lesperance	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 1-18 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-18 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent # 6,229,513 ("Nakano et al.") in view of U.S Patent # 6,356,260 ('Montalbo").

As for claims 1 and 6, Nakano et al. teach a controller 170, including control signals containing the display timing signal DTMG from the graphic controller 180, from a parallel to a serial form and sends the serial signal to the receiver 160 (Fig.10) corresponding to a system including an image processing part for deciding a timing format of an image data and generating a control signal for the image data; an interface unit Fig.1 (100) corresponding to a control board including a power supply part for converting the constant-voltage of the power output part into a predetermined voltage level; reference voltages V5-V9 from circuit 123 (Fig.7) corresponding to a gray scale generating part for generating a gray scale voltage using the predetermined voltage

level of the voltage converting part; gate electrode drive voltage generator Fig.1 (124) corresponding to a gate voltage generating part for gray scale a gate on/off voltage using the predetermined voltage level of the voltage converting part, and signal line (131) corresponding to a transmission line for transmitting the encoded image data and the control signal; the gate drivers Fig.1 (140) corresponding to a first connecting member having a data driver for generating a column signal when the image data, the control signal and the gray scale voltage are applied; the drain drivers Fig.1 (130) corresponding to a second connecting member having a scan driver for generating a scan signal when the control signal and the gate on/off voltage are applied; and liquid display panel Fig.1 (10) corresponding to a flat panel for forming a picture using the scan signal and the column signal. An A/D converter is well known in the art and there is novelty about it Accordingly, Nakano et al. teach all the claimed limitations as recited in claims 1 and 6 with the exception of providing an encoder.

However, Montalbo teach the multiplexed pixel data is transmitted together with the pixel clock which is converted into a RSDS clock signal by RSDS transmit block 560 corresponding to an encoder for encoding into an RSDS specification.

It would have been obvious to utilize the converted RSDS clock signal as taught by Montalbo in the liquid crystal display disclosed by Nakano et al. because this would allow a multiplexed data bus to convey video data into a video display system so as to reduce power consumption and electromagnetic interference.

As for claims 2 and 7, Nakano et al. teach a low voltage decoder (ig.8 (279) corresponding to a first decoding means for decoding the data and the control signal of

the data; a shift register Fig.7 (153) corresponding to a first register means for temporarily storing the data decoded by the first decoding means; and a shift register 153 in a control circuit 152 of the drain driver 130 generates a data fetch signal for an input register 154 based on a clock D4 or D5 for latching display data inputted from the display control unit 110, and outputs the data fetch signal to the input register 154 (column 9, lines 61-65) corresponding to a first signal processing means for generating and outputting a column signal using the data stored in the first register means, the control signal and the gray scale voltage.

As for claims 3 and 8, Nakano et al. teach the 2n originally ordered display data transmitted..... (column7, lines 9-17) and the clock signals D4, D5, which is the same frequency as that of the display data, are transmitted alternately to the groups A and B of the drain drivers 130.... (column 7, lines 33-42) corresponding to the data and the control signal are transmitted in a mixed signal within a single channel, are decoded by the first decoding means, are divided to be stored at a first register and a second register of the first register means, and are output to the first signal processing means.

As for claim 4 and 9, Nakano et al. teach (Fig.7) with a data bus 134 which is separately transmitted from the clock signal D1 and alternating signal M from signal line 135 corresponding to the data and the control signal are separately transmitted through respective corresponding channels, the level shifters 156 convert the voltage levels of display data to higher levels and the high voltage signal decoders 278 and low voltage signal decoders 279 are both formed of high break-down MOS transistors (column 11, lines 4-8) corresponding to are respectively decoded by a first decoder and

a second decoder of the first decoding means, the storage register B (155) and the level shifter (156) corresponding to are divided to be stored at a third register and a fourth register of the first register means, and are output to the first signal processing means.

As for claims 5 and 10, Nakano et al. teach the high voltage and low voltage decoders Fig.8 (261) corresponding to a second decoding means for decoding the control signal; the input registry B Fig.7 (154) corresponding to a second register means for temporarily storing the control signal decoded by the second decoding means; and the display control unit outputs a frame start instruction signal to the gate drivers 140 through a signal line 142, and outputs a shift clock signal G1 to sequentially selecting each gate signal line G of the liquid crystal panel 10 to gate drivers 140 through a signal line 141 for every one horizontal scan period (column 6, lines 50-56) corresponding to a second signal processing means for generating a scan signal using the control signal stored in the second register means and the gate on/off voltage.

As for claim 11, Nakano et al. teach a plurality of drain signal lines (data lines) Fig.1 (130) corresponding to a flat panel having a plurality of data lines, gate signal line Fig.1 (140) corresponding to a plurality of scan lines formed in the matrix configuration; Each pixel is disposed within an area defined by two adjacent first signal lines (drain signal lines D or gate signal lines G) and two adjacent second signal lines (gate signal lines G or drain signal lines D) intersecting therewith (column 5, lines 27-30) corresponding to a system including an image signal processing part; a power supply circuit Fig.1 (120) corresponding to a power output part; an interface unit (100) corresponding to the control board including a gray scale (reference voltages V5-V9

from circuit 123) part; a gate electrode drive voltage generator (124) corresponding to a gate voltage generating part; gate and drain signals (130 and 140) corresponding to power supply part and connected to the flat panel display with a plurality of connecting members.

As for claim 12, Nakano et al. teach a liquid crystal display (TFT) Fig.1 (10).

As for claim 13, Montalbo teaches a timing controller Fig.3c (330c) where some differential data lines are connected to the flat panel display corresponding to the plurality of connecting members apply the RSDS signals to the corresponding column driver integrated circuit.

As for claim 14, Montalbo teaches the two Repeat signals can be transmitted as conventional CMOS signals using TTL levels (Figs.7 and 8) corresponding to a plurality of column driver integrated circuits convert RSDS signals into TTL signal.

As for claim 15, Montalbo teaches the RLP signal can be transmitted as a TTL level signal or any other means appropriate in a flat panel display system (column 7, lines 58-60) corresponding to when the TTL is converted into a column signal and output to the plurality of data lines.

As for claim 16, Montalbo teaches the two Repeat signals can be transmitted as conventional CMOS signals using TTL levels (column 10, lines 43 and 44) corresponding to the first and second decoder connected to the transmission channel and to a control signal transmission channel; pixel data in next pixel register block 910 and current pixel register block 920 (Fig.9) corresponding to first and second register in electrical communication for temporarily storing the TTL signals.

As for claim 17, Montalbo teaches data latches 608a corresponding to the first shift register outputs signals to a data latch.

As for claim 18, Montalbo teaches a shift register 202 which performs a control function, data latches 606a and a local storage for storing the last different color pixel (column 10, lines 63-66) corresponding to a buffer.

Response to Amendment

Applicant's arguments filed 5-27-2003 have been fully considered but they are not persuasive. The applicant argued that the prior art used, Nakano et al., fails to teach an encoder for encoding the image data and the control signal output from the image processing part into a RSDS specification. Examiner agrees with the applicant but has found a new prior that reads on the limitation. The new prior art, Montalbo, teaches that data over the transmission can be converted RSDS to eliminate the noise or EMI. Therefore, the rejection is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (703) 308-6413. The examiner can normally be reached on from Monday to Friday between 8:OOAM and 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709 .

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Art Unit 2674

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Date 9-3-2003